INTERFACE NECTAR ETHERNET

1. Introduction

This note discribes the functionalities of the new NECTAR electronics board.
This board is composed of 16 independant electronics channels.
Each channel is composed of one amplifier, a SAM channel, an ADC channel and a FIFO buffer.
The FIFO buffers are embedded in a Altera Cyclone III FPGA.

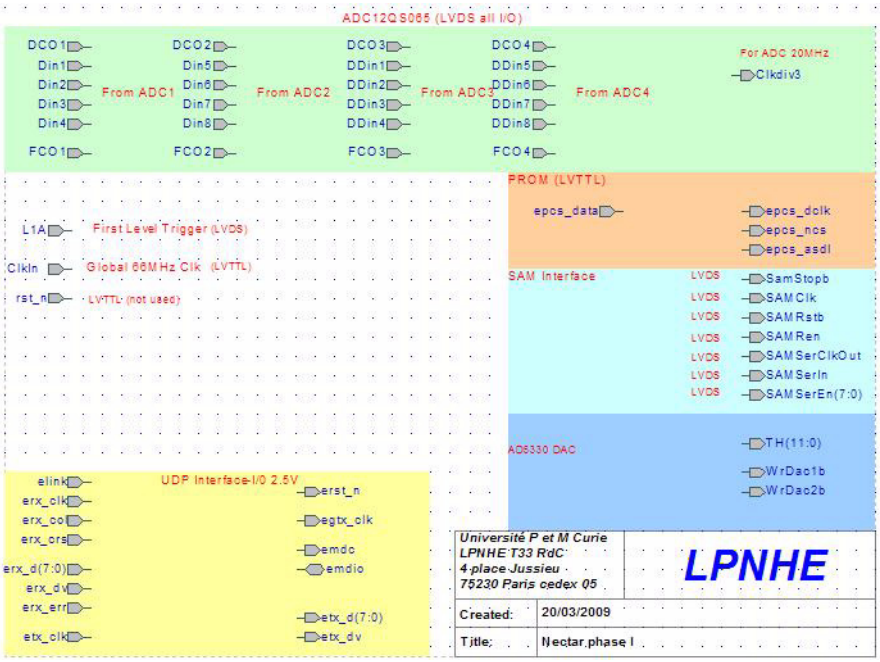

Figure 1.1

2. Software programmation

2.1. GEDEK core programmation

The interface use the following IP Address: 192.168.1.18 and different ports:
port 0x04D3 internal register interface
port 0x04D2 for the reference design board
The internal register interface is used to define different internal parameters:

Address	Functionality	Access	Reset Value
0x00	FPGA Board MAC Address (32 LSB)	R/W	Generic Dependent
0x01	FPGA Board IP Address	R/W	Generic Dependent
0x02	Destination MAC Address (32 LSB)	R/W	0x66322E2A
0x03	Destination MAC Address (16 MSB)	R/W	0x00000019
0x04	Destination IP Address	R/W	0xC0A801CF
0x05	Reserved	N/A	N/A
0x06	Reserved	N/A	N/A
0x07	Reserved	N/A	N/A
0x08	Reserved	N/A	N/A
0x09	Reserved	N/A	N/A
0x0A	Virtual Uart Link UDP Port Number (When Available)	R/W	0x00000017
0x0B	Reserved	N/A	N/A
0x0C	Reserved	N/A	N/A
0x0D	Reserved	N/A	N/A
0x0E	Reserved	N/A	N/A
0x0F	Reserved	N/A	N/A

For example the destination IP Address: 0xC0A801CF must be interpreted after hex to dec conversion as C0.A8.01.CF:

C0 -192
A8 -168
01 -01
CF -207

In order to access the previous register bank, we must send the following UDP frames word1 et word2:

word 1 (32-bit): [31:24]=Addr
[23:16]=Command
[15:08]=0xFF
[07:00]=0x00

Command 0x04 Read register
0x08 Write register

and in the case of a write command
word2 (32-bit): data to be written in the register at Addr

2.2. Reference design programmation

This part of the programmation is the user part and gives access to the data.
5 blocks are used to configure the slow control of the board:
All the following words are 32-bit.

CntrlSlc is used to program the threshold for the pixel (Thrshld1 8-bit), the threshold for the pixel sum (Thrshld2 8-bit) and the common mode voltage VMC (12-bit).

0000AAAA
00007E0C
[0000Thrshld1] [0000Thrshld2] [0000VMC]
0000AAAA
--

CntrlSAMReg is used to program the internal SAM registers CDR1, CDR2 and TestFCR
0000AAAA
00007E3E
[0000CDR1] [0000CDR2] [000000TestFCR]
0000AAAA
--
CNTRLSamDac is used to program the 32 internal SAM DACs
0000AAAA
00007E3A
0000DAC1L0 0000DAC2L0 0000DAC1L1 0000DAC2L1 0000DAC1L2 0000DAC2L2 0000DAC1L3 0000DAC2L3
0000DAC1L4 0000DAC2L4 0000DAC1L5 0000DAC2L5 0000DAC1L6 0000DAC2L6 0000DAC1L7 0000DAC2L7
0000DAC1L8 0000DAC2L8 0000DAC1L9 0000DAC2L9 0000DAC1LA 0000DAC2LA 0000DAC1LB 0000DAC2LB
0000DAC1LC 0000DAC2LC 0000DAC1LD 0000DAC2LD 0000DAC1LE 0000DAC2LE 0000DAC1LF 0000DAC2LF
-- 0000AAAA
--
CNTRLSamNd is used to define the delay pointer Nd
0000AAAA
00007E3C
000000Nd
0000AAAA

CNTRLDAQ is used to define the DAQ parameters
0000AAAA
00007E30
000000XX [Nf][x][Q/Sampls][T0][TOT] [8][1][1][1][1]
0000AAAA

The 2 following blocks are used to receive data in either charge mode or sampling mode.

DAQCHARGE
0000AAAA
0000EEE0
0000Evtcounter (16-bit)
0000Data block (16 x 16-bit)
0000AAAA

DAQSAMPLE
0000AAAA
0000EEE3
0000Evtcounter (16-bit)
0000Data block (16 x Nf x 16-bit)
0000AAAA

2.3. EPROM programmation

The design allows to program through ethernet the EPCS FPGA EPROM. This EPROM is used to store the internal FPGA code necessary to operate.

For this purpose, the internal register addresses are used:

x40 EPCSRdRamRdData
x41 EPCSRdRamRdAddress
x42 EpcsStartAddress
x43 reserved for data writing
x44 EPCSStatus