INTERFACE NECTAR ETHERNET

1. Introduction

This note discribes the functionalities of the new NECTAR electronics board. This board is composed of 16 independent electronics channels.

Each channel is composed of one amplifier, a SAM channel, an ADC channel and a FIFO buffer.

The FIFO buffers are embedded in a Altera Cyclone III FPGA.

)S all I			
DCO 1 Din 1 Din 2 Din 2 Din 3 Din 4 Din 4	DC02D- Din5D- Din6D- Din7D- Din8D-	m ADC2	DCO3 DDin1 DDin2 DDin3 DDin4			m A		CO4 Din5 Din6 Din6 Din7 Din7 Din8 Din8 D-		For ADC 20MHz -DClkdiv3
FCO1D-	FCO2D-		FCO3				F	CO4 <u>—</u> —		
		- 608-19	3 A.		0.80	-53	-	PROM (LVTTL)		
				21 2 35 2	8 12 6 14		::::::	epos_dataD+-		-Depos_dolk
	el Trigger (LVDS)		1.0			20				-Depos_nos -Depos_asdi
ikin D- Global 86	MHz Clk (LVTTL)	1001 94	3.12	8	8	.87	1000	SAM Interface	LVDS	Sam Stopb
rst_nD+ · LVTTL (not	used) · · · · ·	1001.00	92 - 93 1	2.	1	15	100		LVDS	-SAM Cik
			13 IX	• •	8 8 3	-22	-2033-		LVDS	-SAM Rstb
			3.13			-30			LVDS	-SAM Ren -SAM SerCikOut
		8 9668 68 9 6666 68					5,67,8		LVDS	-SAM Serin
		1 1002 10			6 55				LVDS	-SAM SerEn(7:0)
		-	10 10	12. 5		-23	12:51			
			12 12	1911				AD5330 DAC		-TH(11:0)
14 14 14 14 14 14 14 14 14 14 14 14 14 1			197 - 197				2005	ADDODU DAG		
elinkD-	UDP Interface-I/0 2	.5V	st n				2025			
erx_cik erx_co		-Deg	and a second		23	-30	200			
erx ors		-Dea	DK_OIK		88	1	Univer	sité P et M Curie		
		emdc emdio etx d(7:0)			2 3	1	LPNHE T33 RdC			
x_d(7:0) erx_dv —								Jussieu Paris cedex 05	LF	INFIE
erx_errD-					2	Created:		d: 20/03/2009	10.00	
etx clk		-Deb			•		Title:	Nectar phase I		

Figure 1.1

2. Software programmation

2.1. GEDEK core programmation

The interface use the following IP Address: 192.168.1.18 and different ports: port 0x04D3 internal register interface port 0x04D2 for the reference design board The internal register interface is used to define different internal parameters:

Address	Functionality	Access	Reset Value
0x00	FPGA Board MAC Address (32 LSB)	R/W	Generic Dependent
0x01	FPGA Board IP Address	R/W	Generic Dependent
0x02	Destination MAC Address (32 LSB)	R/W	0x66322E2A
0x03	Destination MAC Address (16 MSB)	R/W	0x00000019
0x04	Destination IP Address	R/W	0xC0A801CF
0x05	Reserved	N/A	N/A
0x06	Reserved	N/A	N/A
0x07	Reserved	N/A	N/A
0x08	Reserved	N/A	N/A
0x09	Reserved	N/A	N/A
0x0A	Virtual Uart Link UDP Port Number (When Available)	R/W	0x00000017
0x0B	Reserved	N/A	N/A
0x0C	Reserved	N/A	N/A
0x0D	Reserved	N/A	N/A
0x0E	Reserved	N/A	N/A
0x0F	Reserved	N/A	N/A

For example the destination IP Address: 0xC0A801CF must be interpreted after hex to dec conversion as C0.A8.01.CF:

C0 -192 A8 -168 01 -01 CF -207

In order to access the previous register bank, we must send the following UDP frames word1 et word2:

word 1 (32-bit):	[31:24]=A	ddr		
	[23:16]=Co	ommand		
	[15:08]=0x	xFF		
	[07:00]=0x00			
Command	0x04	Read register		
	0x08	Write register		

and in the case of a write command word2 (32-bit): data to be written in the register at Addr

2.2. Reference design programmation

This part of the programmation is the user part and gives access to the data. 5 blocks are used to configure the slow control of the board: All the following words are 32-bit.

CntrlSlc is used to program the threshold for the pixel (Thrshld1 8-bit), the threshold for the pixel sum (Thrshld2 8-bit) and the common mode voltage VMC (12-bit).

```
0000AAAA
00007E0C
[0000Thrshld1] [0000Thrshld2] [0000VMC]
0000AAAA
--
```

CntrlSAMReg is used to program the internal SAM registers CDR1, CDR2 and TestFCR 0000AAAA 00007E3E [0000CDR1] [0000CDR2] [000000TestFCR] 0000AAAA --CNTRLSamDac is used to program the 32 internal SAM DACs 0000AAAA 00007E3A 0000DAC1L0 0000DAC2L0 0000DAC1L1 0000DAC2L1 0000DAC1L2 0000DAC1L3 0000DAC2L3 0000DAC1L0 0000DAC2L4 0000DAC1L5 0000DAC2L5 0000DAC1L6 0000DAC2L2 0000DAC1L3 0000DAC2L3 0000DAC1L8 0000DAC2L8 0000DAC1L5 0000DAC2L9 0000DAC1L6 0000DAC2L6 0000DAC1L7 0000DAC2L8 0000DAC1LC 0000DAC2LC 0000DAC1LD 0000DAC2LD 0000DAC1LE 0000DAC2LE 0000DAC1LF 0000DAC2LF -- 0000AAAA --CNTRLSamNd is used to define the delay pointer Nd

0000AAAA 00007E3C 000000Nd 0000AAAA

CNTRLDAQ is used to define the DAQ parameters 0000AAA 00007E30 000000XX [Nf][x][Q/Sampls][T0][TOT] [8][1][1][1][1] 0000AAAA

The 2 following blocks are used to receive data in either charge mode or sampling mode.

DAQCHARGE

0000AAAA 0000EEE0 0000Evtcounter (16-bit) 0000Data block (16 x 16-bit) 0000AAAA

DAQSAMPLE

0000AAAA 0000EEE3 0000Evtcounter (16-bit) 0000Data block (16 x Nf x 16-bit) 0000AAAA

2.3. EPROM programmation

The design allows to program through ethernet the EPCS FPGA EPROM. This EPROM is used to store the internal FPGA code necessary to operate.

For this purpose, the internal register addresses are used:

- x40 EPCSRdRamRdData
- x41 EPCSRdRamRdAddress
- x42 EpcsStartAddress
- x43 reserved for data writing
- x44 EPCSStatus