

## *Procedure*

This section provides know-how procedures the CALICE team share.

- **Ideal topology:**

PC (or ODR made by UK)

- LDA: Link Data Agregator (made by UK)
- (x2)
  - \* DCC (made by LLR)
  - \* (x10)
    - DIFF (made by LLR or LAPP)
    - (x9)

- **Power supply:**

- ASU: ?
- CCC: home made Alim (UK)
- DCC: 5v, from 3mA 18W max Alim
- LDA: 12V-0.5A and 5.5V-1A (ok from PC Alim)
- DIF ECAL (Xilinx): 3.3v-0.5A (ok from PC Alim)
- DIF DHCAL (Altera): 5v-0.5A (ok from PC Alim)

**Note:** PC Alim is switched on by linking the green and black input of main motherboard cable.

- 4 kinds of links are used (identified by the Ethernet Type 809, 810, 811):

- PC to CCC: RS232 (working but not used) reach throught an ACKSYS COM/ETH convertor.
- PC (or ODR) to LDA: Ethernet Gigabit on rj45 (Ethernet but not IP)
- CCC to LDA: HDMI plugged from dedicated LDA Mezzanine
- LDA to DCC: Home made Ethernet over HDMI (no MAC address, see the documentation section)
- DCC to DIF: Home made Ethernet over HDMI (no MAC address, see the documentation section)
- DIF to ASU: 100+ pins connector

**Notes:**

- HDMI runs at 50 MHz that implies 40 Mb/s due to 8b/10b Encoding.
- Question is: may LDA be replaced by standards Eternet Switch ?
- With the actual firmware, LDA needs the CCC to work (6 red leds).
- `uint16_t ODR_Data_and_PAD[0]` ; is a meta attribute for the following data in memory.
- ODR (not used) state of the art (`odr_server`) is describe in *svn/calice/online-sw/trunk/doc/odr-calice.txt*.

- **Hosts**

- `poltestcalice`: old DHCAL test bed (svn, xilinx 11, pyserdiag)

- polcaldaq: DHCAL+ECAL test bed (svn, xilinx 11+12, pyserdiag, optical eth)
- poldhcp45: SC55 for soft devel (svn, libLDA)
- poldhcp54: new DHCAL test bed (svn, xilinx 11+12, pyserdiag) ?
- pollinmc2: SC55 for soft devel (svn, libLDA, XDAQ)
- polcalslc: SC55 pizza box for XDAQ devel (svn, libLDA, Xdaq)
- pollinbtc: ECAL cosmic test bed (svn, libLDA, pyserdiag via virtual machine)
- polntnr: Nicoas Roche's laptop
- polsmtp: smtp
- polynet: intranet
- polzope: intranet
- llrforge: */pwhash/*
- llroffice: *ELog*
- polui0[1-7]: gateways
- lyoac[19,20,26]: IPNL gateways reachable only via polui0x
- lxplus.cern.ch: Cern gateway