Approach

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This section remind the actual status and provide the methods we use to update them.

1 Firwares versions

1.1 LDA

There is 3 FPGA but only main is checkable via slow control.

• startup: ?

• main: v23.02.2011 => limited to 112Mb/s

• hdmi: ?

Using the libLDA, you should read the LDA version from log:

INFO: LDA version: 03-23-2011

1.2 DCC

Using the libLDA, you should read the DCC versions from log:

INFO: DCC@1 version: 18-07, id=16, status=4

1.3 DIFv

We are now working with v2.2l version. This may be change at compilation.

	v1	v1.2	v2	v2.2l
Fifo fast cod missing		X	?	?
Provides fake headers				X
Inverse rng data orders				X

2 Jumpers

Jumpers:

• LDA:

- j5: none

```
- j22: 3v3
```

- j31: 2v5
- j38: 0001 (marked side)
- switchs:

1 2 3 4 5 6 7 8

original: 1 0 1 1 0 1 1 1 modified: 1 0 1 0 1 1 1 1

• DIFF ECAL:

- j1: none
- j2: none
- j3: 011
- j4: 011

• DIFF DHCAL:

- j6: none
- j8: none

3 Leds

- LDA:
 - 6 red leds: ok
- DCC:
 - link: green=ok
 - clock: orangex2=ok
- DIFF ECAL:
 - green led = not programmed at power on
 - additionnal red led: blinking and next lited: ok

4 Inventory

- CCC:
 - **3**: LLR
 - **5**: LPNL
 - **6**: LLR
- LDA:
 - 9: 5e:70:0c:d2:51:0a
 - 10: 5e:70:0c:d2:79:68 Low HDMI mezzanine
 - 11: 5e:70:0c:d2:5e:95 Low HDMI mezzanine
 - **12**: 5e:70:0c:d2:77:e8
 - **20**: 5e:70:0c:d2:78:34

- **21**: 5e:70:0c:d2:54:fe
- **25**: 5e:70:0c:d2:5c:d6
- \bullet DCC:
 - **1**:
- DIFF ECAL:
 - **3**: LLR
 - **4**: LLR
 - **5**: LLR Warning
 - **6**: LLR
 - **7**: LLR
 - **13**: LLR
 - **14**: LLR
 - **15**: LLR
 - **16**: LLR
 - **17**: LLR
- DIFF DHCAL:
 - **5**: LPNL
 - **8**: LLR
 - **25**: LPNL
 - **27**: LLR
 - **30**: LLR
 - **35**: LLR
 - **36**: LLR
 - **40**: LLR
 - **154**: LPNL
- ASU DHCAL:
 - **7**: LLR